

# **Computer Architecture Research Challenges 2005-2015**

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February 15, 2005**

# Extreme Integration

- How best to use 10B transistors?
- Many-sequencer machines
  - Many cores, many threads (100s-1000s)
  - Limits of TLP/MLP, emerging workloads
  - Interconnect, caches, memory, I/O issues
- Key challenges
  - Power, die area, thermal, design methodology
  - OS scalability, SW migration, program model
  - Parallel program tuning/debugging, support for Si validation, support for legacy OS/SW

*Evolutionary Process ...*

# Resilient Architecture

- Ensure functionality, reliability and usability in light of unpredictable, unexpected and undesirable effects
- Accommodate wide parameter variations and restricted physical design styles
- Tolerate latent bugs, transient errors, gradual errors, intermittent faults, degradation faults, and security breaches
- Provide architecture support for system crash avoidance, transparent reboot, instantaneous resume, and human error tolerance

*Paradigm Shift ...*

# Extreme Packaging

- Leverage 3D die/wafer stacking technology
- “System on stack” (SOS)
  - DRAM, NVRAM, cache hierarchy, specialized cores, GPUs, MMPIUs, etc.
  - RC and power mitigation while scaling on performance, functionality, and integration
- Modular system design framework
  - Die-to-die “open” interfaces
  - Reusable die as IP building block
  - Heterogeneous technologies

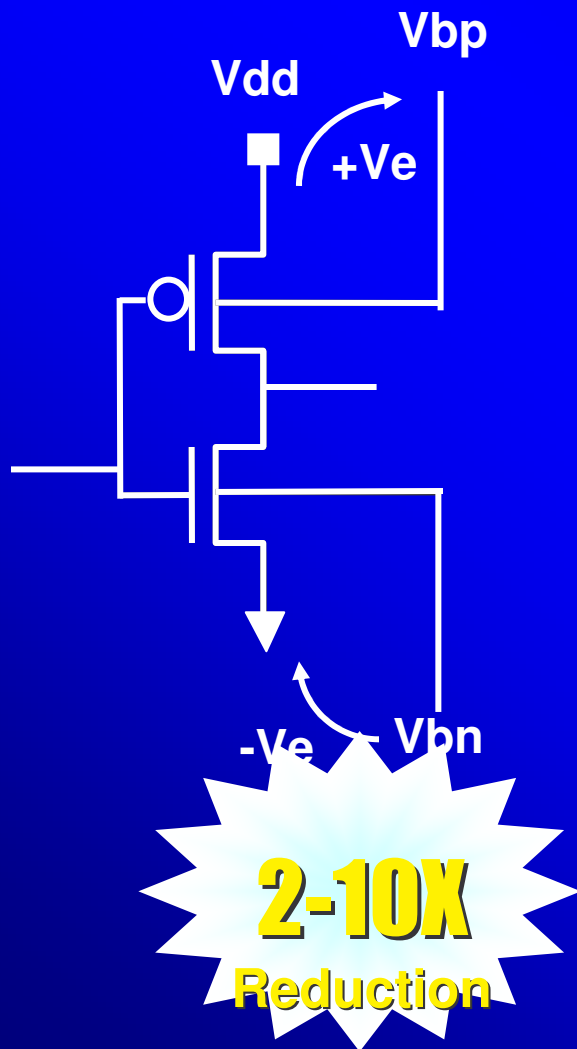
*Exploit & Revolutionize ...*

# Summary of Key Areas

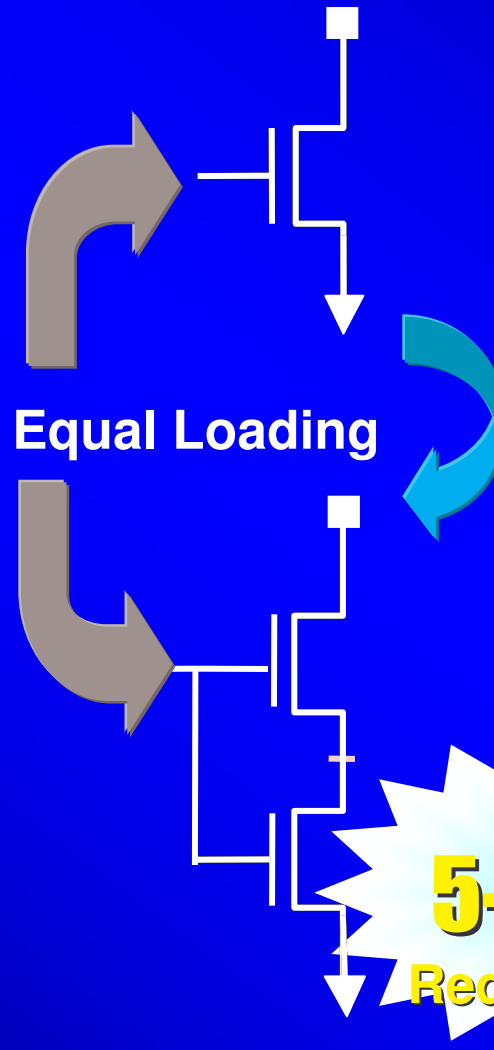
- Extreme integration
- Resilient architecture
- Extreme packaging

# Leakage Control

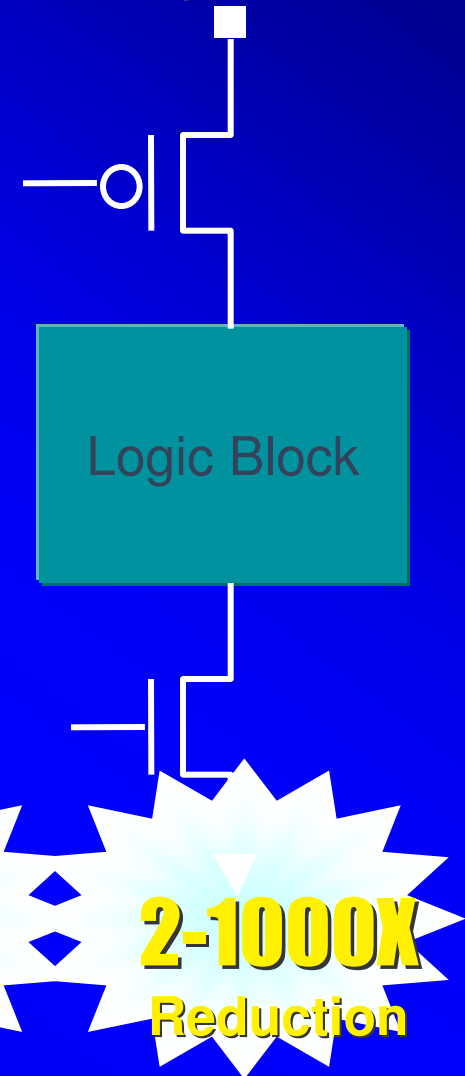
Body Bias



Stack Effect



Sleep Transistor



# Variation-tolerant Design

