

## HPCA-12 Final Program

### Saturday Feb. 11th 2006

08:00am-08:30am	<b>Breakfast</b>
08:30am-05:00pm All Day Events*	<b>Tutorial T2: The Design and Implementation of the TRIPS EDGE Architecture</b> Doug Burger (Univ of Texas at Austin), Steve Keckler (Univ of Texas at Austin), Kathryn McKinley (Univ of Texas at Austin)
	<b>Workshop W1: HPCRI-2: Workshop on High Performance Computing Reliability Issues</b> Padma Apparao (Intel Labs), Greg Averill (Digital Enterprise Group)
	<b>Workshop W2: WMPI-2006: Workshop on Memory Performance Issues</b> John Carter (University of Utah), Lixin Zhang (IBM Austin Research Lab)
01:00pm-05:00pm Afternoon Events*	<b>Tutorial T1: Microprocessor Memory Array Circuits for Architects</b> Shih-Lien Lu (Microarchitecture Research, Intel Labs), Nam Sung Kim (Circuit Research, Intel Labs), Steven Hsu (Circuit Research, Intel Labs)

### Sunday Feb. 12th 2006

08:00am-08:30am	<b>Breakfast</b>
08:30am-05:00pm All Day Events*	<b>Workshop W4: CAECW-9: Workshop on Computer Architecture Evaluation using Commercial Workloads</b> Lieven Eeckhout (Ghent University), Ravi Iyer (Intel Labs)
	<b>Workshop W5: INTERACT-10: Workshop on Interaction between Compilers and Computer Architectures</b> Sangyeun Cho (Univ. of Pittsburgh), Gyungho Lee (Univ. of Illinois at Chicago)
	<b>Workshop W6: PPEC-3: Workshop on Productivity and Performance in High-End Computing</b> Ram Rajamony (IBM, Program Chair), Nick Nystrom (PSC), Philip Johnson (Univ. of Hawaii), Vijay Saraswat (IBM), Larry Votta (Sun)
	<b>Workshop W7: WARFP-2006: Workshop on Architecture Research using FPGA Platforms</b> Arvind (MIT), Krste Asanovic (MIT), Derek Chiou (UT Austin), James Hoe (CMU), Christoforos Kozyrakis (Stanford), Shih-Lien Lu (Intel)
	<b>Workshop W8: RIDMS-1: Workshop on Real Time, Interactive, and Digital Media Supercomputing</b> Ashwini K. Nanda (IBM TJ Watson Research Center)
01:00pm-05:00pm Afternoon Events*	<b>Workshop W3: WISA-2006: Workshop on IntroSpective Architectures</b> Hsien-Hsin S. Lee (Georgia Tech), Trevor Mudge (Michigan), Milos Prvulovic (Georgia Tech)
06:00pm-08:00pm	<b>HPCA Reception at hotel</b>

\* All workshops and tutorials above will take place simultaneously with following breaks.  
10:00am-10:30am: break, 12:00pm-01:00pm: lunch (provided), 03:00pm-03:30pm: break

### Monday Feb. 13th 2006

08:00am-08:30am	<b>Breakfast</b>
08:30am-08:45am	<b>Welcome:</b> Craig Chase, Yale Patt and Chita R. Das
08:45am-09:45am	<b>Keynote I: New Architectures for a New Biology</b> David E. Shaw, D.E. Shaw & Co.
09:45am-10:15am	<b>Break</b>
10:15am-11:45am	<b>SESSION 1: Chip Multiprocessors (CMPs)</b> Chair: Josep Torrellas (UIUC)
	<b>BulletProof: A Defect-Tolerant CMP Switch Architecture</b> Kypros Constantinides (University of Michigan), Stephen Plaza (University of Michigan), Jason Blome (University of Michigan), Bin Zhang (University of Texas), Valeria Bertacco (University of Michigan), Scott Mahlke (University of Michigan), Todd Austin (University of Michigan), Michael Orshansky (University of Texas)
	<b>CMP Design Space Exploration Subject to Physical Constraints</b> Yingmin Li (University of Virginia), Benjamin Lee (Harvard University), David Brooks (Harvard University), Zhigang Hu (IBM T.J.Watson), Kevin Skadron (University of Virginia)
	<b>Exploiting Parallelism and Structure to Accelerate the Simulation of Chip Multi-processors</b> David A. Penry (Princeton University), Daniel Fay (University of Colorado at Boulder), David Hodgdon (University of Colorado at Boulder), Ryan Wells (Princeton University), Graham Schelle (University of Colorado at Boulder), David I. August (Princeton University), Dan Connors (University of Colorado at Boulder)
11:45am-01:15pm	<b>Lunch (provided)</b>
01:15pm-02:45pm	<b>SESSION 2: Processor Architecture</b> Chair: James C. Hoe (CMU)
	<b>An Approach for Implementing Efficient Superscalar CISC Processors</b> Shiliang Hu (Univ. of Wisconsin – Madison), Ilhyun Kim (Intel), Mikko H. Lipasti (Univ. of Wisconsin – Madison), James E. Smith (Univ. of Wisconsin – Madison)
	<b>A Decoupled KILO-Instruction Processor</b> Miquel Pericàs (Universitat Politècnica de Catalunya (UPC) & Barcelona Supercomputing Center (BSC)), Adrian Cristal (UPC & BSC), Ruben González (UPC), Daniel A. Jiménez (Rutgers University), Mateo Valero (UPC & BSC)
	<b>Store Vectors for Scalable Memory Dependence Prediction and Scheduling</b> Samantika Subramaniam (Georgia Tech), Gabriel H. Loh (Georgia Tech)
02:45pm-03:15pm	<b>Break</b>

03:15pm-04:45pm	<b>SESSION 3: Parallel Architecture</b> Chair: Ashwini Nanda (IBM T.J. Watson) <b>Dynamic Power-Performance Adaptation of Parallel Computation on Chip Multiprocessors</b> Jian Li (Cornell University), José F. Martínez (Cornell University) <b>Last Level Cache (LLC) Performance of Data Mining Workloads On a CMP – A Case Study of Parallel Bioinformatics Workloads</b> Aamer Jaleel (Intel Corporation), Matthew Mattina (Tilera Corporation), Bruce Jacob (University of Maryland, College Park) <b>Construction and Use of Linear Regression Models for Processor Performance Analysis</b> P. J. Joseph (Indian Institute of Science), Kapil Vaswani (Indian Institute of Science), Matthew J. Thazhuthaveetil (Indian Institute of Science)
04:45pm-05:00pm	<b>Break</b>
05:00pm-06:30pm	<b>Panel: Patenting the Fruits of Academic Research: What are the Implications?</b> Moderator: Rich Belgard Panel members: John Amster, Intellectual Ventures, Bellevue, WA Rich Belgard, Consultant, Saratoga, CA Mike Heim, Heim, Payne & Chorush, LLP, Houston, TX Trevor Mudge, University of Michigan, Ann Arbor, MI Yale Patt, University of Texas, Austin, TX
07:00pm-08:00pm	<b>TCCA Business Meeting</b>
<b>Tuesday Feb. 14th 2006</b>	
08:00am-08:45am	<b>Breakfast</b>
08:45am-09:45am	<b>Keynote II: Chip-multiprocessing and Beyond</b> Per Stenström, Chalmers University of Technology
09:45am-10:15am	<b>Break</b>
10:15am-11:45am	<b>SESSION 4: Energy and Power</b> Chair: Trevor Mudge (Michigan) <b>Probabilistic Counter Updates for Predictor Hysteresis and Stratification</b> Nicholas Riley (UIUC), Craig Zilles (UIUC) <b>Phase Characterization for Power: Evaluating Control-Flow-Based and Event-Counter-Based Techniques</b> Canturk Isci (Princeton University), Margaret Martonosi (Princeton University) <b>DMA-Aware Memory Energy Management</b> Vivek Pandey (UIUC), Weihang Jiang (UIUC), Yuanyuan Zhou (UIUC), Ricardo Bianchini (Rutgers University)
11:45am-01:15pm	<b>Lunch (provided)</b>
01:15pm-02:45pm	<b>SESSION 5: Memory Systems</b> Chair: Qing Yang (University of Rhode Island) <b>Increasing the Cache Efficiency by Eliminating Noise</b> Prateek Pujara (Binghamton University), Aneesh Aggarwal (Binghamton University) <b>Retention-Aware Placement in DRAM (RAPID): Software Methods for Quasi-Non-Volatile DRAM</b> Ravi K. Venkatesan (North Carolina State University), Stephen Herr (North Carolina State University), Eric Rotenberg (North Carolina State University) <b>Completely Verifying Memory Consistency of Test Program Executions</b> Chaiyasit Manovit (Sun Microsystems, Sunnyvale, CA), Sudheendra Hangal (Magic Lamp Software, Bangalore, India)
02:45pm-03:15pm	<b>Break</b>
03:15pm-04:15pm	<b>SESSION 6: Disk and High Performance I/O</b> Chair: Ricardo Bianchini (Rutgers Univ.) <b>Understanding the Performance-Temperature Interactions in Disk I/O of Server Workloads</b> Youngjae Kim (Pennsylvania State University), Sudhanva Gurumurthi (University of Virginia), Anand Sivasubramaniam (Pennsylvania State University) <b>High Performance File I/O for The Blue Gene/L Supercomputer</b> H. Yu (IBM TJ Watson Research Centre), R. K. Sahoo (IBM TJ Watson Research Centre), C. Howson (IBM TJ Watson Research Centre), G. Almási (IBM TJ Watson Research Centre), J. G. Castañón (IBM TJ Watson Research Centre), M. Gupta (IBM TJ Watson Research Centre), J. E. Moreira (IBM System & Technology Group), J. J. Parker (IBM System & Technology Group), T. E. Engelsiepen (IBM Almaden Research Center), R. B. Ross (Argonne National Lab), R. Thakur (Argonne National Lab), R. Latham (Argonne National Lab), W. D. Gropp (Argonne National Lab)
04:15pm-04:30pm	<b>Break</b>
04:30pm-06:00pm	<b>SESSION 7: Industrial Perspectives on Challenges for Next-Generation Computer Systems</b> (Invited presentation) Chair: Mazin Yousif (Intel) <b>Platform Design Challenges with Many cores</b> Raj Yavatkar (Intel Fellow) <b>System IO Network Evolution - Closing Requirement Gaps</b> Renato Recio (IBM Distinguished Engineer) <b>The Next Roadblocks in SOC Evolution: On-Chip Storage Capacity and Off-Chip Bandwidth</b> Philip Emma (Manager, IBM)

06:30pm-10:30pm	<b>Conference Banquet</b>
<b>Wednesday Feb. 15th 2006</b>	
08:00am-09:30am	<b>SESSION 8: Fault-Tolerant Architecture and Security</b> Chair: Vijaykrishnan Narayanan (Penn State Univ.) <b>ReViveI/O: Efficient Handling of I/O in Highly-Available Rollback-Recovery Servers</b> Jun Nakano (UIUC), Pablo Montesinos (UIUC), Kourosh Gharachorloo (Google), Josep Torrellas (UIUC), <b>Reducing Resource Redundancy for Concurrent Error Detection Techniques in High Performance Microprocessors</b> Sumeet Kumar (Binghamton University), Aneesh Aggarwal (Binghamton University) <b>InfoShield: A Security Architecture for Protecting Information Usage in Memory</b> Weidong Shi (Georgia Tech), Joshua B. Fryman (Intel), Guofei Gu (Georgia Tech), Hsien-Hsin S. Lee (Georgia Tech), Youtao Zhang (University of Pittsburgh), Jun Yang (University of California, Riverside)
09:30am-09:45am	<b>Break</b>
09:45am-11:15am	<b>SESSION 9: Hardware/Software Tradeoffs</b> Chair: Doug Burger (UT Austin) <b>CORD: Cost-effective (and nearly overhead-free) Order-Recording and Data race detection</b> Milos Prvulovic (Georgia Tech) <b>Software-Hardware Cooperative Memory Disambiguation</b> Ruke Huang (Univ. of Rochester), Alok Garg (Univ. of Rochester), Michael Huang (Univ. of Rochester) <b>LogTM: Log-based Transactional Memory</b> Kevin E. Moore (University of Wisconsin-Madison), Jayaram Bobba (University of Wisconsin-Madison), Michelle J. Moravan (University of Wisconsin-Madison), Mark D. Hill (University of Wisconsin-Madison), David A. Wood (University of Wisconsin-Madison)
11:15am-11:30am	<b>Break</b>
11:30am-01:00pm	<b>SESSION 10: Multi-Threaded Systems</b> Chair: Milos Prvulovic (GATECH) <b>The Common Case Transactional Behavior of Multithreaded Programs</b> JaeWoong Chung (Stanford University), Hassan Chafi (Stanford University), Chi Cao Minh (Stanford University), Austen McDonald (Stanford University), Brian Carlstrom (Stanford University), Christos Kozyrakis (Stanford University), Kunle Olukotun (Stanford University) <b>Speculative Synchronization and Thread Management for Fine Granularity Threads</b> Alex Gontmakher (Technion), Avi Mendelson (Intel), Assaf Schuster (Technion), Gregory Shklover (Technion) <b>Efficient Instruction Schedulers for SMT Processors</b> Joseph Sharkey (SUNY Binghamton), Dmitry Ponomarev (SUNY Binghamton)