

Call for Papers

HPCRI: 2nd Workshop on High Performance Computing Reliability Issues

To be held in conjunction with
[the 12th International Symposium on High Performance Computer
Architecture \(HPCA-12\)](#)

Omni Austin Hotel Downtown, Austin, Texas
February 11-15, 2006

Workshop Chairs:

Padma Apparao
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Organizing / Program Committee:

Mootaz Elnozahy	IBM
Ravi Iyer	UIUC
Jarek Nieplocha	PNL
Sartaj Sahni	U. of Florida
Darius Tanksalvala	HP

Important Dates:

Abstract	Dec 5 th '05
Paper Submission	Dec 15 th '05
Notification of Accept	Jan 6 th '06
Camera Ready Due	20 th Jan '06

Conference Website:

<http://www.hpcaconf.org/hpca12/>

For more information, please send
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Application demands and trends in the hardware and software industry have necessitated the development of High Performance Computing Systems with high availability and reliability. Clusters and grids are a cost-effective way of solving high performance computing needs and are built by using thousands of commodity systems that are geographically distributed and provide fast, dependable and reliable access to data and resources. Thus reliability of the underlying platform is essential to high performance computing. The design trends in the circuit technology with smaller die sizes and faster clock speeds have made the components more prone to random errors and crosstalk. Fault tolerant approaches in the hardware/micro architecture are necessary to mitigate component level errors. The workshop will address the reliability and availability needs for HPC and the integration of these techniques into enterprise and technical server systems. Recent developments and future direction will be presented in order to share and stimulate ideas for developing highly reliable systems for performing high performance tasks. The workshop will have several areas of focus: trends in rates of errors and types of errors, error detection and recovery mechanisms, fault prediction, and fault-driven provisioning of large scale systems.

Topics of interest include (but are not limited to):

- Error Detection, Mitigation and Recovery
 - Error Types and Rates
 - Characterization of Errors (e.g., radiation-induced, hard, intermittent, etc.)
 - Detection Mechanisms
 - Monitoring Tools and Techniques
 - Error Detection Latencies
 - Performance Impacts / Overhead
 - Techniques for Error Recovery
- Reliability Design
 - Caches/memory architecture
 - Interconnect architecture
- Fault Prediction
- Fault Modeling
- Self-healing / Autonomics for error handling in cluster/grid environments
- Hardware Redundancy Techniques to decrease error rates

Paper Submission Information:

We welcome submissions in the form of abstracts (< 1 page) and short papers (5-7 pages). Please e-mail your submissions (preferably in pdf) to padmashree.k.apparao@intel.com and gregory.s.averill@intel.com