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David Kaeli, *Northeastern Univ.*

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Josep Torrellas, *Univ. of Illinois at Urbana-Champaign*  
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#### Local Arrangements

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#### Finance Chair

Shubu Mukherjee, *Intel*

#### Registration Chair

Srilatha Manne, *Intel*

#### Tutorial Chair

Gus Uht, *Univ. of Rhode Island*

#### Workshop Chair

Antonio Gonzalez, *UPC, Barcelona*

#### Publications Chair

Kevin Skadron, *Univ. of Virginia*

#### Publicity Chair

Andreas Moshovos, *Univ. of Toronto*

### Workshops Saturday, February 2, 2002

**8:30am - 5:00pm:**  
**CAECW-02: Computer Architecture Evaluation Using Commercial Workloads**  
Russell Clapp, IBM  
Kimberly Keeton, Hewlett-Packard Laboratories  
Ashwini Nanda, IBM TJ Watson Research Center

**8:20am - 5:00pm:**  
**PACS'02: Power-Aware Computer Systems**  
Babak Falsafi, CMU  
T. N. Vijaykumar, Purdue

**8:45am - 4:30pm:**  
**SAN-1: Workshop on Novel Uses of System Area Networks**  
Mark Heinrich, Cornell  
Evan Speight, Cornell

### Workshops & Tutorial Sunday, February 3, 2002

**8:30am - 12:00pm:**  
**Tutorial: Designing Cluster-based Data Centers: Emerging Technologies and Research Challenges**  
Dhabaleswar K. Panda, The Ohio State University  
Hemal Shah, Intel

**8:30am - 5:00pm:**  
**NSC-1: Workshop on Non-Silicon Computing**  
Nick Carter, UIUC  
Seth Copen Goldstein, CMU

**8:55am - 6:15pm:**  
**NP-1: Workshop on Network Processors**  
Patrick Crowley, Univ. of Washington  
Mark Franklin, Washington Univ. in St. Louis  
Haldun Hadimioglu, Polytechnic Univ.  
Peter Z. Onufryk, IDT

**9:00am - 5:00pm:**  
**INTERACT-6: Interaction between Compilers and Computer Architecture**  
Gyungho Lee, Iowa State

**7:00pm: Reception, Sonesta Skyline Suites**

The conference is held at the:  
Royal Sonesta Hotel Boston  
Five Cambridge Parkway  
Cambridge, MA 02142  
Tel: (617) 806-4200  
Fax: (617) 806-4232

8th Annual International Symposium on

# High-Performance Computer Architecture

*Royal Sonesta Hotel*  
*Cambridge, MA, Feb. 2 - 6, 2002*



## Conference Program



COMPAQ

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## Main Program

Monday, February 4, 2002

8:45 Introductory remarks from General and Program chairs

9:00 Keynote speaker:

Timothy Chou, President, Oracle.com  
*The Software Industry: Ten Lessons for Long Life*

10:00 Break

### 10:30 ENERGY AND THERMAL MANAGEMENT I

Session chair: A.Sivasubramaniam, *Pennsylvania State Univ.*

**Microarchitectural Simulation and Control of di/dt-induced Power Supply Voltage**

Ed Grochowski, Dave Ayers, and Vivek Tiwari

**Control-Theoretic Techniques and Thermal-RC Modeling for Accurate and Localized Dynamic Thermal Management**

Kevin Skadron, Mircea Stan, and Tarek Abdelzaher

**Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling**

G. Semeraro, G. Magklis, R. Balasubramonian, D. H. Albonesi, S. Dwarkadas, and M. L. Scott

12:00 Lunch, Skyline Suites

### 1:30 MULTITHREADING

Session chair: Yiannakis Sazeides, *University of Cyprus*

**Learning Cross-Thread Violations in Speculative Parallelization for Scalable Multiprocessors**

Marcelo Cintra and Josep Torrellas

**Thread-Spawning Schemes for Speculative Multithreading**

Pedro Marcuello and Antonio Gonzalez

**Improving Value Communication for Thread-Level Speculation**

J. Gregory Steffan, Christopher B. Colohan, Antonia Zhai and Todd C. Mowry

3:00 Break

### 3:30 PANEL DISCUSSION

**What will have the greatest impact in 2010:  
The processor, the memory, or the interconnect?**

Moderator: Timothy Mark Pinkston (USC)

Panelists: *Anant Agarwal (MIT), Bill Dally (Stanford), Jose Duato (UPV, Spain), Bob Horst (Horst Technology Research), Yale Patt (Texas at Austin), T. Basil Smith (IBM)*

6:00 BANQUET, New England Aquarium

Buses leave at 6:00pm in front of the Royal Sonesta and will begin to return around 9:45pm

## Tuesday, February 5, 2002

9:00 POTPOURRI

Session chair: Shubu Mukherjee, *Intel*

**Reverse Tracer: A Software Tool for Generating Realistic Performance Test Programs**

M. Sakamoto, L. Brisson, A. Katsuno, A. Inoue, and Y. Kimura

**Tuning Garbage Collection in an Embedded Java Environment**

G. Chen, R. Shetty, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, and M. Wolczko

9:00 MEMORY-AWARE SCHEDULING

Session chair: Mahmut Kandemir, *Pennsylvania State Univ.*

**Fine-grain Priority Scheduling for Memory-Intensive Applications**

Zhichun Zhu, Zhao Zhang, and Xiaodong Zhang

**A New Memory Monitoring Scheme for Memory-Aware Scheduling and Partitioning**

G. Edward Suh, Srinivas Devadas, and Larry Rudolph

10:00 Break

### 10:30 ENERGY AND THERMAL MANAGEMENT II

Session chair: Margaret Martonosi, *Princeton University*

**The Minimax Cache: An Energy-Efficient Framework for Media Processors**

O. S. Unsal, I. Koren, C. Mani Krishna, and C. Andras Moritz  
**Using Complete Machine Simulation for Software Power Estimation: The SoftWatt Approach**

S. Gurumurthi, A. Sivasubramaniam, M. J. Irwin, N. Vijaykrishnan, M. Kandemir, T. Li and L. K. John

**Exploiting Choice in Resizable Cache Design to Optimize Deep-Submicron Processor Energy-Delay**

Se-Hyun Yang, M. D. Powell, B. Falsafi and T. N. Vijaykumar

12:00 Lunch, Skyline Suites

### 1:30 LATENCY TOLERANCE AND CACHES

Session chair: Steve Lumetta, *UIUC*

**Non-vital Loads**

Ryan Rakvic, Bryan Black, Deepak Limaye, and John P. Shen

**Let's Study Whole-Program Cache Behaviour Analytically**  
Xavier Vera and Jingling Xue

**Two Memory Latency-Tolerance Approaches for Itanium Processors: Out-of-Order Execution vs. Speculative Precomputation**

P. Wang, H. Wang, J. Collins, E. Grochowski, R. Kling, and J. Shen

**Quantifying Load Stream Behavior**

Suleyman Sair, Timothy Sherwood, and Brad Calder

3:30 Break

Parallel Sessions

### 4:00 SPECULATION AND PREDICTION

Session chair: Brad Calder, *University of California at San Diego*

**Modeling Value Speculation**

Yiannakis Sazeides

**The FAB Predictor: Using Fourier Analysis to Predict the Outcome of Conditional Branches**

Martin Kampe, Per Stenstrom, and Michel Dubois

**Power Issues Related to Branch Prediction**

D. Parikh, K. Skadron, Y. Zhang, M. Barcella, and M. Stan

### 7:30 WORK-IN-PROGRESS

Organizers: Bruce Childers (University of Pittsburgh), Koji Inoue (Fukuoka University), Sally A. McKee (University of Utah), Martin Schulz (Technische Universitat Munchen).

Dinner on your own

## Wednesday, February 6, 2002

9:00 Keynote speaker:

David A. Patterson,  
Pardee Chair of Computer Science  
University of California at Berkeley

*Recovery Oriented Computing:  
A New Research Agenda for a New Century*

10:00 Break

### 10:30 MULTIPROCESSOR SYSTEMS

Session chair: Babak Falsafi, *Carnegie Mellon University*

**Bandwidth Adaptive Snooping**

Milo M. K. Martin, Daniel J. Sorin, Mark D. Hill, and David A. Wood

**CableS: Thread Control and Memory Management Extensions for Shared Virtual Memory Clusters**

Peter Jamieson and Angelos Bilas

**User-Level Communication in Cluster-Based Servers**

E. V. Carrera, S. Rao, L. Iftode, and R. Bianchini

### 10:30 PIPELINING AND MICROARCHITECTURE

Session chair: Gary Tyson, *University of Michigan*

**Using Internal Redundant Representations and Limited Bypass to Support Pipelined Adders and Register Files**

Mary D. Brown and Yale N. Patt

**Loose Loops Sink Chips**

Eric Borch, Eric Tune, Srilatha Manne, and Joel Emer

**Evaluation of a Multithreaded Architecture for Cellular Computing**

Calin Cascaval, Jose Castanos, Luis Ceze, Monty Denneau, Manish Gupta, Derek Lieber, Jose Moreira, Karin Strauss, and Henry S. Warren, Jr.

12:00 End of Conference

Parallel Sessions