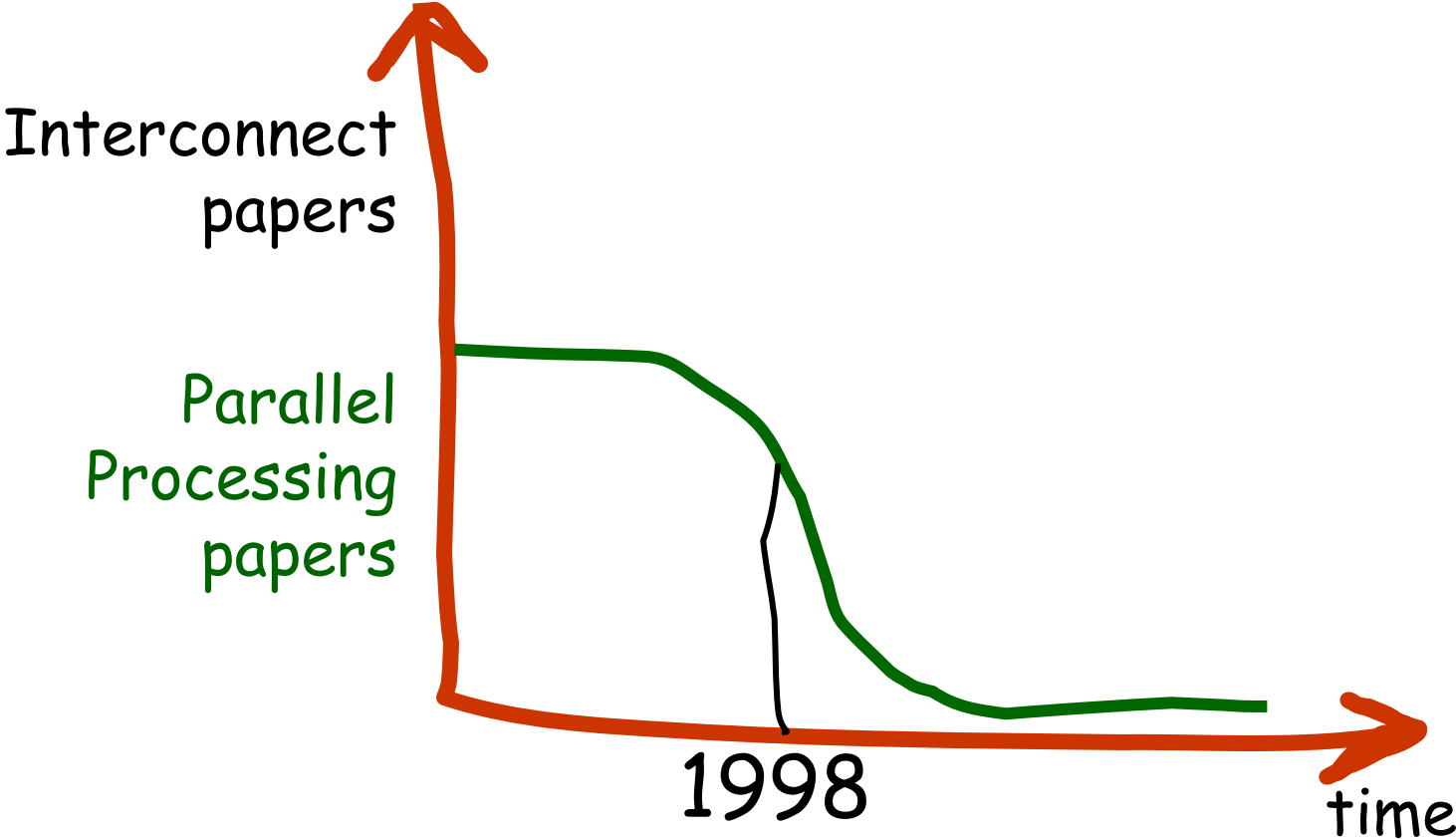


# HPCA Panel

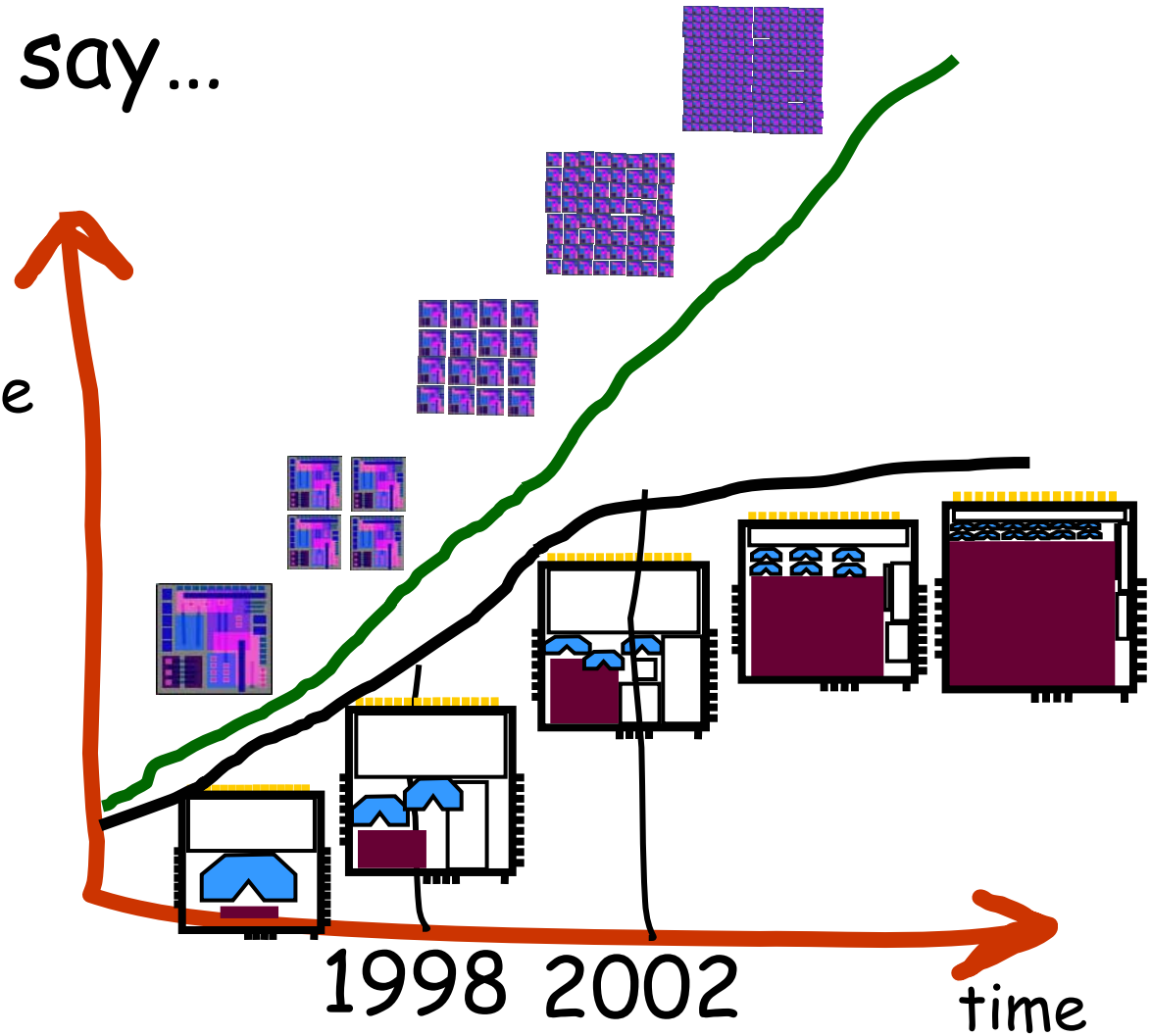
Anant Agarwal  
MIT

Pinkston said...

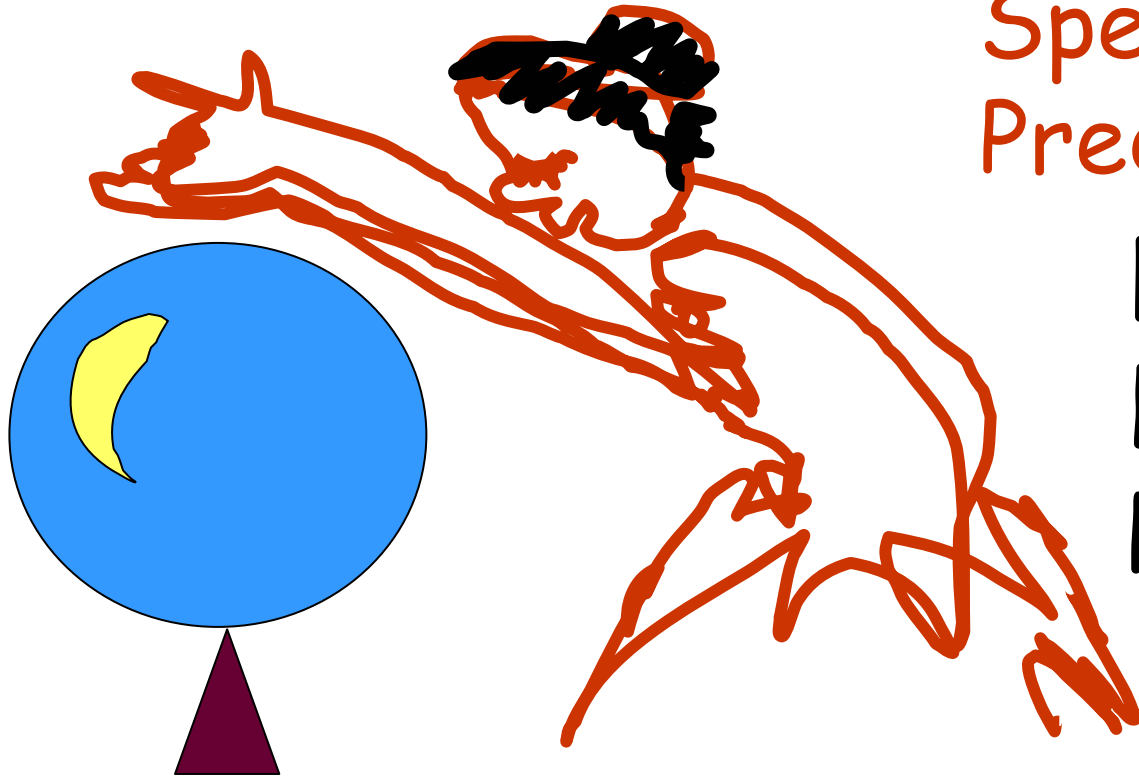


# Dally will say...

Performance



Flat liners will say...



Predict  
Speculate  
Predicate

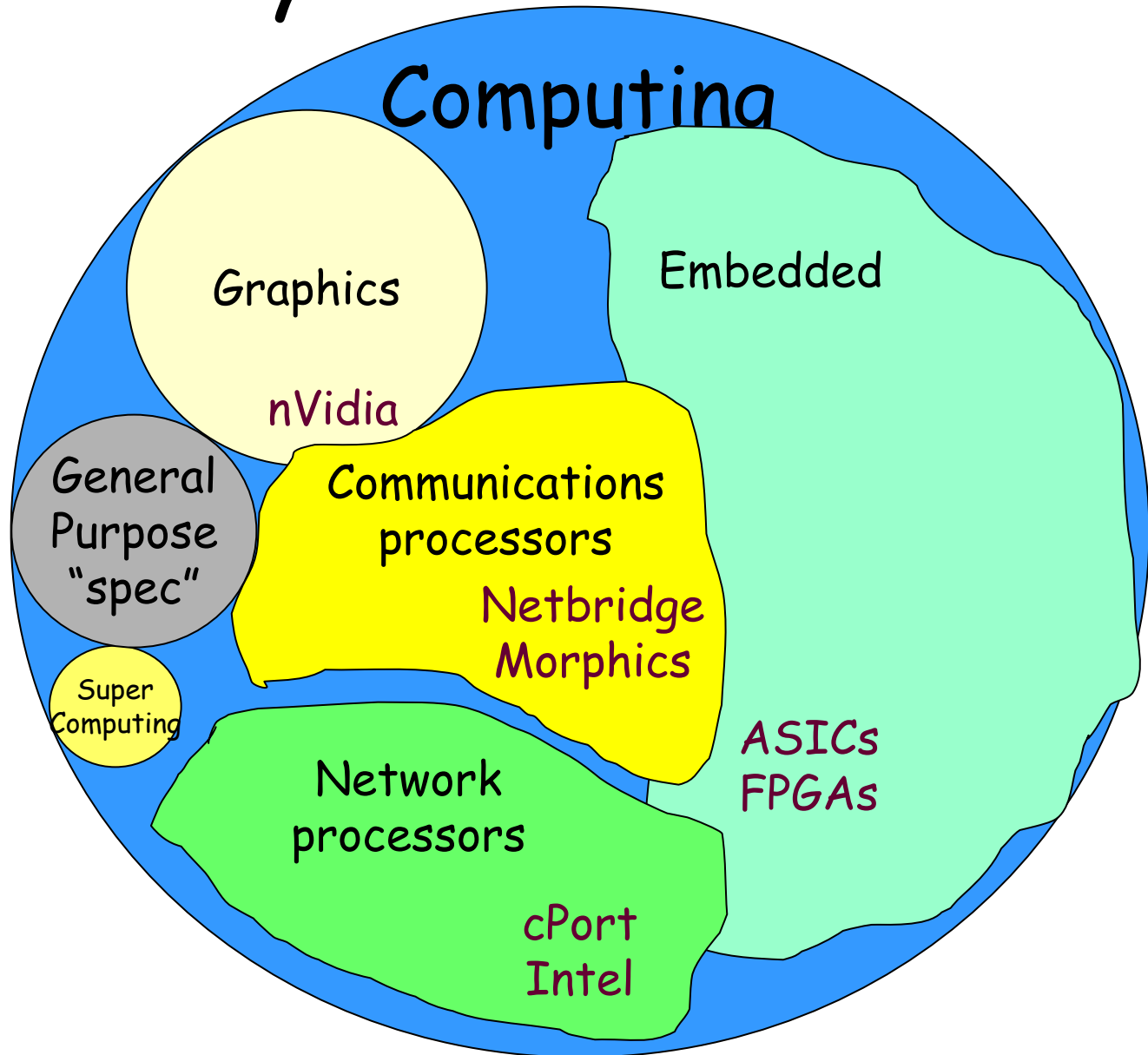
Faith  
Hope  
Pray...

# Parallel processing's two body blows...

Sequential juggernaut -- Ending...

Focus on supercomputing -- ??????

# Agarwal says...



# Agarwal says...

## Computing

The action is here...

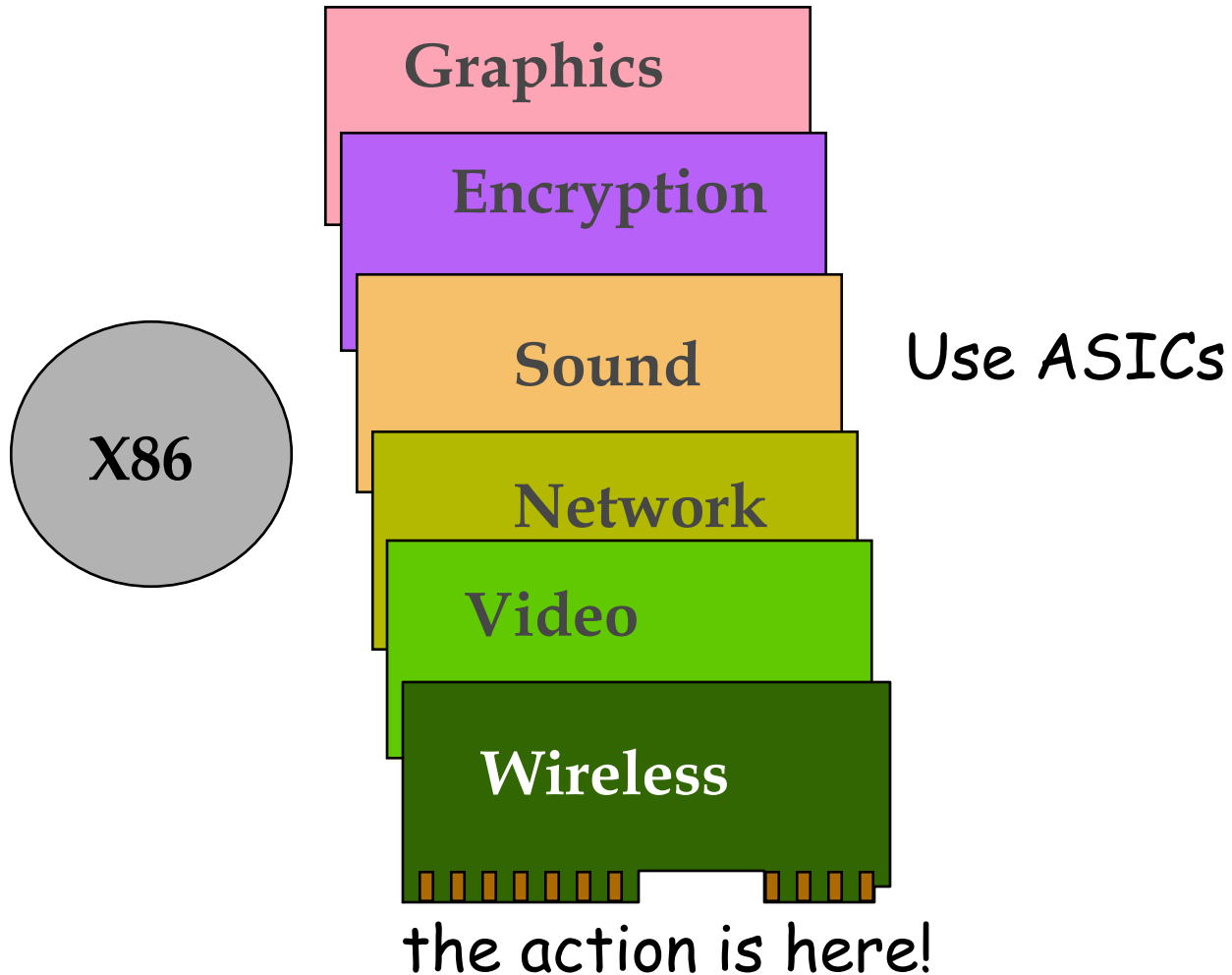
General  
Purpose  
"spec"

Super  
Computing

Streaming data  
Highly parallel (often, pipeline)  
Need energy efficiency  
Need huge I/O bandwidth

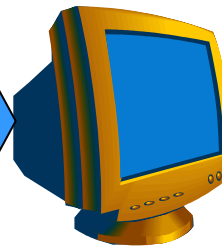
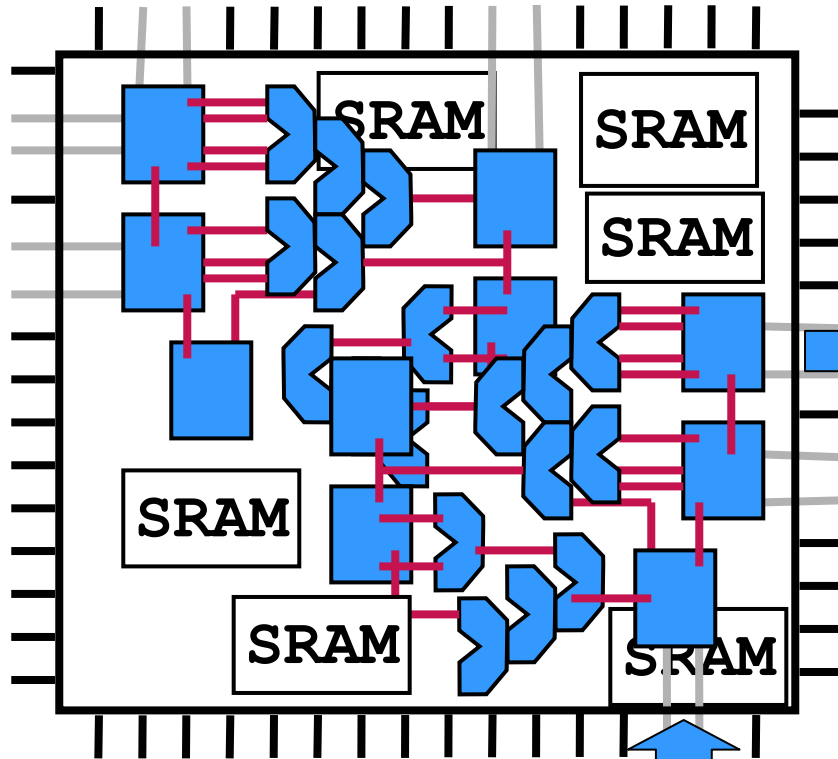
Challenge: Build the 21<sup>st</sup> century  
general purpose processor

# Even inside your PC...

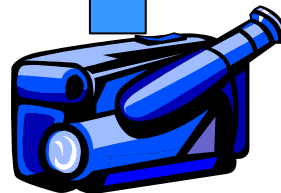


# Lesson from ASICs

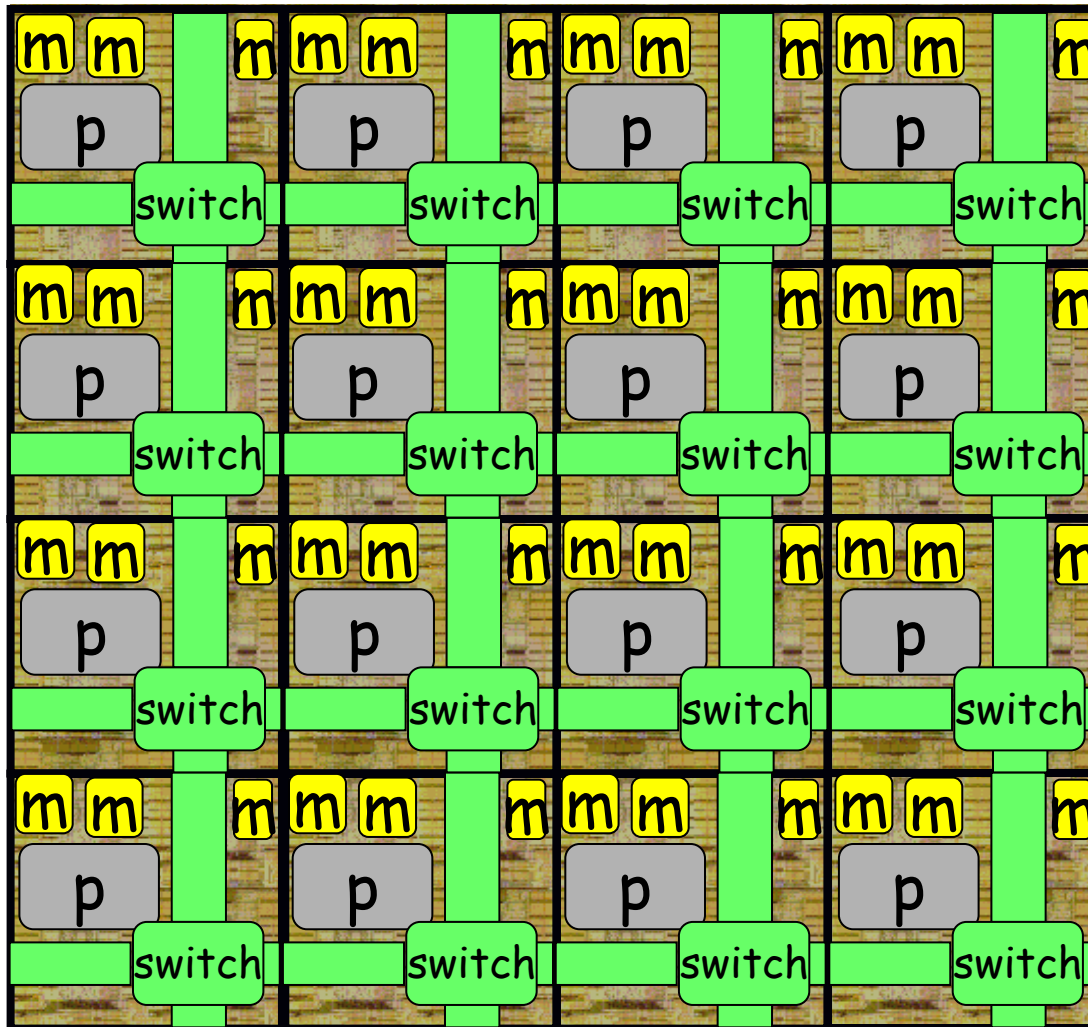
Lots of ALUs,  
local mems, I/O  
*Specialized wiring  
localizes action*



But...  
Done by hand  
Not programmable



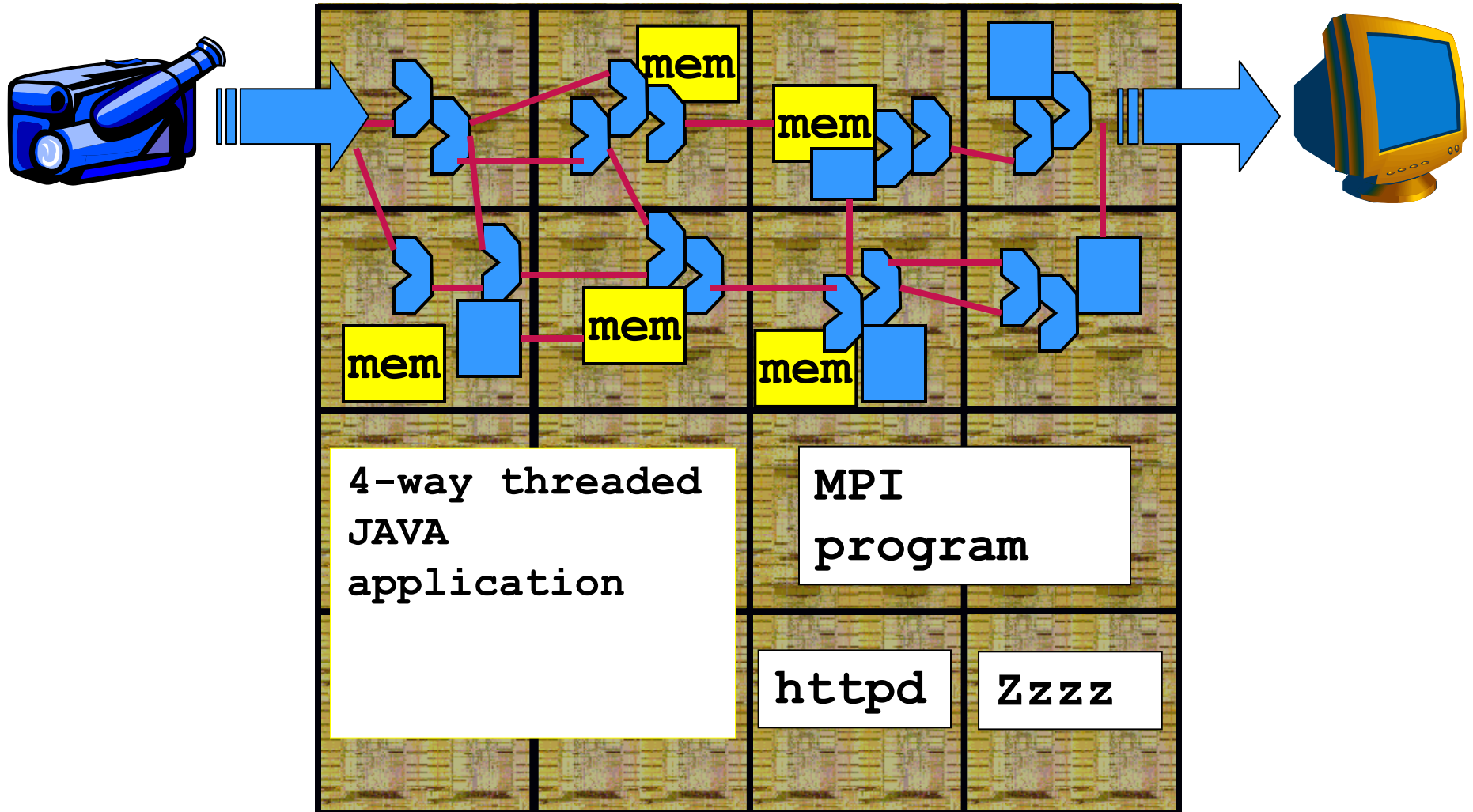
# Imagine this architecture...



Programmable  
switch  
exposes the  
interconnect (the  
important stuff)  
to the software

Like an FPGA for 21<sup>st</sup> century computing

# Where the ISA includes *switch* ops...



... so wiring/interconnect can be programmed

# The battle lines are being drawn...



Several groups working on interconnect exposed architectures:

U Illinois FlexRAM

UT Austin's Grid Proc Arch

Stanford's Smart Memories

CMU PipeWrench

MIT's Raw

... join the fight. Don't be a flatliner!

# Juicy research questions...



What is the right interconnect ISA

What is the interconnect architecture

Can it support streaming and GP apps

What is the architecture of the logic unit

Does it even matter

What is the right balance - how big is a tile

Dynamic versus static interconnect

Application studies - how close to ASICs

Audio, video, networking app studies

Interconnect deadlock

Support for bit-level configurability

What is the memory architecture

What is the I/O architecture

Scalability studies

Oh, and compilers and runtime software systems

# Perspective...

Performance  
of cache  
coherence  
schemes

